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--REMARKS --

Oath. In the Non-Final Office Action, Examiner Steelman objected to the declaration as being defective. To obviate this objection, Applicants are concurrently filing an amended declaration with signatures from all of the inventors.

Claims. In the Non-Final Office Action, Examiner Steelman rejected pending claims 1-16 on various grounds. The Applicants respond to each rejection as subsequently recited herein, and respectfully requests reconsideration and further examination of the present application:

    A.   Examiner Steelman rejected claims 13 and 14 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,513,146 B1 to *Yonezawa* et al.

The Applicants have thoroughly considered Examiner Steelman's remarks concerning the patentability of claims 13 and 14 over *Yonezawa*. The Applicants have also thoroughly read *Yonezawa*. To warrant this 102(e) rejection of claims 13 and 14, *Yonezawa* must show each and every limitation of independent claim 13 in as complete detail as in contained in independent claim 13. See, MPEP §2131. The Applicants respectfully traverse this 102(e) rejection of claims 13 and 14, because *Yonezawa* fails to teach or suggest an "determining the relative power consumption of the plurality of compound Single Instruction/Multiple Data instructions incorporating one or more of the micro-operations based on the relative energy values of the incorporated micro-operations" as recited in amended independent claim 13.

Withdrawal of the rejection of amended independent claim 13 under 35 U.S.C. §102(e) as being anticipated by *Yonezawa* is therefore respectfully requested

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Claim 14 depends from amended independent claim 13. Therefore, dependent claim 14 includes all of the elements of amended independent claim 13. It is therefore respectfully submitted by the Applicants that dependent claim 14 are allowable over *Yonezawa* for at least the same reasons as set forth herein with respect to amended independent claim 13 being allowable over *Yonezawa*. Therefore, withdrawal of the rejection of dependent claim 14 under 35 U.S.C. §102(e) as being anticipated by *Yonezawa* is therefore respectfully requested.

B.   Examiner Steelman rejected claim 1 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No 4,574,358 B1 to *Scallon*

The Applicants have thoroughly considered Examiner Steelman's remarks concerning the patentability of independent claim 1 over *Scallon* The Applicants have also thoroughly read *Scallon*. To warrant this 35 U.S.C. §103(a) rejection of independent claim 1, all the claim limitations recited in independent claim 1 must be taught or suggested by the *Scallon*. See, MPEP §2143. The Applicants respectfully traverse this §103(a) rejection of independent claim 1, because *Scallon* teaches away from "combining said at least two Single Instruction/Multiple Data operations to execute in a single instruction cycle to thereby yield the compound Single Instruction/Multiple Data instruction" as recited in independent claim 1.

Generally, the basis of the present invention is to combine related vector operations into a single compound SIMD instruction, in order to perform as many operations on the data per instruction cycle as possible to reduce the required energy for instruction and data word fetches, without any significant (negative) hardware impact as seen in *Scallon*.

Specifically, *Scallon* teaches the use of a complex instruction, which as known in the art is a very long instruction word ("VLIW") consisting of multiple instructions sequentially ordered as words/fields to form the VLIW whereby the words/fields are individually sent to different hardware units (e.g., ALUs) in parallel during an execution of the VLIW. By contrast, a compound SIMD instruction as recited in independent claim 1 and defined by the present application consists of a combination of multiple SIMD operations into a single word that results in a more compact and more efficient instruction as compared to a VLIW. As opposed to *Scallon*, the present invention does not require that differing portions of the compound Single Instruction/Multiple Data instruction be individually sent to different hardware units (e.g., ALUs) in parallel during an execution of the compound SIMD instruction.

Particularly, *Scallon* recites "The instruction is actually a complex instruction in which certain fields are fed to ALU8a, and other fields fed to the remaining ALUs until the last field is fed to the last ALU 8n. Thus, in effect, separate instructions are sent to each execution unit. ... Each execution unit operates independently to process the data appearing in the data stream in accordance with the operational codes dictated by the instruction field which it sees." See, *Scallon* at column 4, lines 46-56). This is in direct contrast to the present application, which utilizes compound SIMD instructions (sending the same operational code to each ALU) to reduce power consumption and instruction size requirements. The net effects of these compound SIMD instruction techniques result in a significant power and cost savings over VLIW and compressed-VLIW architectures since smaller amounts of instruction and data need to be fetched from memory and/or register files.

Withdrawal of the rejection of independent claim 1 under 35 U.S.C. §103(a) as being unpatentable over *Scallon* is therefore respectfully requested.

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    C.   Examiner Steelman rejected claims 2 and 3 under 35 U.S.C. §103(a)
as being unpatentable over U.S. Patent No. 4,574,358 to *Scallon* in
view of U.S. Patent No. 6,513,146 B1 to *Yonezawa* et al.

Claims 2 and 3 depends from independent claim 1. Therefore, dependent
claims 2 and 3 include all of the elements of independent claim 1. It is therefore
respectfully submitted by the Applicants that dependent claims 2 and 3 are allowable
over *Scallon* for at least the same reasons as set forth with respect to independent
claim 1 being allowable over *Scallon*. Therefore, withdrawal of the rejection of
dependent claims 2 and 3 under 35 U.S.C. §103(a) as being unpatentable over *Scallon*
in view of *Yonezawa* is respectfully requested.

    D.   Examiner Steelman rejected claims 4-16 under 35 U.S.C. §103(a) as
being unpatentable over U.S. Patent No. 4,574,358 to *Scallon* in
view of U.S. Patent No. 6,513,146 B1 to *Yonezawa* et al. and in
further view of "SPONSOR'S FEATURE - DSP PROCESSORS
Power and efficiency Architectures for this Century's applications"
to *Oed* et al.

Claims 4-12 depend from independent claim 1. Therefore, dependent claims
4-12 include all of the elements of independent claim 1. It is therefore respectfully
submitted by the Applicants that dependent claims 4-12 are allowable over *Scallon* in
view of *Yonezawa* and in further view of *Oed* for at least the same reasons as set forth
with respect to independent claim 1 being allowable over *Scallon*. Furthermore,
Scallon, *Yonezawa* and *Oed* in combination fails to teach or suggest "wherein the
compound Single Instruction/Multiple Data instruction includes conditional
operations on element of a data vector" as recited in independent claim 10, "wherein
the compound Single Instruction/Multiple Data instruction includes a vector

conditional negate and add operation" as recited in independent claim 11, and
"wherein the compound Single Instruction/Multiple Data instruction includes a vector
select and viterbi shift left operation" as recited in independent claim 12. In
particular, *OED* teaches using a coprocessor to perform specific processing (such as
Viterbi processing), but they do not teach a specific compound SIMD instruction to
implement such processing.

Therefore, withdrawal of the rejection of dependent claims 4-12 under 35
U.S.C. §103(a) as being unpatentable over *Scallon* in view of *Yonezawa* and in further
view of *Oed* is respectfully requested.

> E.   Examiner Steelman rejected claim 15 under 35 U S.C. §103(a) as
>   being unpatentable over U.S. Patent No. 6,513,146 B1 to *Yonezawa*
>   et al. in view of U.S. Patent No. 4,574,358 to Scallon

The Applicants have cancelled claim 15 herein. Withdrawal of the rejection
of dependent claim 15 under 35 U.S.C. §103(a) as being unpatentable over *Yonezawa*
in view of *Scallon* is therefore respectfully requested.

> F.   Examiner Steelman rejected claim 16 under 35 U S.C. §103(a) as
>   being unpatentable over U.S. Patent No 6,513,146 B1 to *Yonezawa*
>   et al.

The Applicants have thoroughly considered Examiner Steelman's remarks
concerning the patentability of independent claim 16 over *Yonezawa*. The Applicants
have also thoroughly read *Yonezawa*. To warrant this 35 U.S.C. §103(a) rejection of
independent claim 16, all the claim limitations recited in independent claim 1 must be
taught or suggested by *Yonezawa*. See, MPEP §2143. The Applicants respectfully

traverse this §103(a) rejection of independent claim 16, because *Yonezawa* fails to teach or suggest "simulating a software algorithm including one or more compound Single Instruction/Multiple Data instructions of a reduced instruction set computing type" as recited in amended independent claim 16.

Withdrawal of the rejection of independent claim 16 under 35 U.S.C. §103(a) as being unpatentable over *Yonezawa* is therefore respectfully requested.

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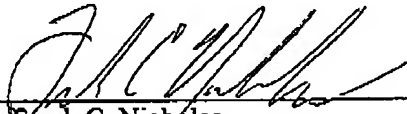Serial No.: 10/082,900
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SUMMARY

The Applicants respectfully submit that pending claims 1-14 and 16 as listed herein fully satisfy the requirements of 35 U.S C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested. If any points remain in issue that may best be resolved through a personal or telephonic interview, Examiner Steelman is respectfully requested to contact the undersigned at the telephone number listed below.

Dated: **April 12, 2005**

Respectfully submitted,
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